CURRICULUM VITAE

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- **Educational qualification**
  1. Ph.D. from IIT Bombay in Microelectronics specialization of Electrical Engineering Department, with total CPI of 6.48 for the 58 credits (2019).
  2. B.E. from IET, DAVV Indore in Electronics & Telecommunication Engineering, with total 70.83 % of marks (2006).
  3. Diploma from SVP Indore (RGPV Bhopal) in Electronics with total 80.68 % of marks (2003).

- **Work experience**

1. **December 2014 to August 2018**

   Name of Organization**: National Institute of Solar Energy, Gurgaon**
   Position Held**: Senior Research Scientist**
   Nature of Duties**:**

   - Under skill development division: Preparation of proposals for organizing and conducting international training programs in the field of Solar Energy Technologies and Applications, for the participants from different countries politically connected through India by the following groups:
     - International Technical and Economic Cooperation (ITEC)
     - South Asian Association for Regional Cooperation (SAARC)
     - Indo- African Forum Submit (IAFS)
     - International Solar Alliance (ISA)
   - These training programs were fully funded by Ministry of External Affairs and Ministry of New and Renewable Energy, GoI. Hence the job scope included coordinating with Indian Missions and participants. Also responsible for all the administrative work like logistics and other preparations towards successful completion of the program.
   - Delivered lectures on high efficiency c-Si solar cell technology in the training programs held at the institute.
   - Under SVP Lighting system laboratory: The specific work allotted was to get the large integrating sphere up and running for the SPV light testing.
   - Under Research & Development cell: Coordinated with various meetings held for setting up of material and device characterization laboratory under high-efficiency solar cell with advance structure as passivated emitter rear cell (PERC).

2. **July 2007 to December 2014**
   Name of Organization**: Department of Electrical Engineering, IIT Bombay, Mumbai**
   Position Held**: Teaching Assistance, Research Scholar**
   Nature of Duties**:**

- Teaching assistant (2007-2009): The job scope included assistance in laboratory, assignments and various matters assigned by subject supervisor (subjects like VLSI technology, nanoelectronics, physical electronics and VLSI design).
- Research Scholar (2009-2014):
  - Working towards PhD research in centre for excellence in nanoelectronics (CEN) and national centre for photovoltaic research and education (NCPRE) at IIT Bombay, included working in different systems for the semiconductor device fabrication followed by material and device characterizations. During the time, these laboratories was under establishment phase for high-end tools and systems, hence I did contributed towards setting up of the systems. With the hands-on experience in commissioning of tools like Applied Materials ENDURA PVD and CENTURA Gate stack tool and spectroscopic ellipsometer.
  - The job scope also included assistant to users of laboratory and others for completion of their respective projects.
  - Delivered hands-on training and seminar on systems used for device fabrication and characterization. Volunteered in different conferences and workshops held in departments and also and delivered lectures related to workshops.

3. **July 2006 to July 2007**
   Name of Organization**: Lakshmi Narain College of Technology, Indore**
   Position Held**: Lecturer**
   Nature of Duties**:** Teaching engineering subjects like Digital electronics and Analog electronics, microprocessor.

- **PhD work**

  Topic: Pulsed-DC reactive sputtered aluminum oxide for the surface passivation of crystalline silicon solar cell
  Supervisor: Prof. Anil Kottantharayil

- **Technical experience**
  1. **Fabrication**
     - Proficiency in the theory and operation of the deposition processes like physical vapour deposition (PVD) and chemical vapour deposition (CVD)
     - Experience of working in an industrial deposition systems like Applied Materials ENDURA PVD tool and Applied Materials CENTURA Gate stack tool
     - Experience of working on rapid thermal processing (RTP) tool for optimization of post-deposition processes
     - Knowledge of LPCVD furnace processes
     - Knowledge of thermal evaporator for metal deposition

2. **Electrical Characterization**
   - Trained on C-V and I-V characterizations of MOS capacitor structures in semiconductor characterization tools.
3. **Optical Characterization**
   - Trained on In-house Solar simulator to measure Dark I-V and Light I-V characteristics of solar cells
   - Trained on Life-time tester to measure minority carrier life-time
4. **Physical Characterization**
   - Proficiency in Spectroscopy Ellipsometer measurement
   - Proficiency in cross sectional TEM sample preparation
   - Trained on X-ray reflectivity (XRR) measurements (an attachment to XRD system)
5. **Simulations**
   - SENTAURUS (semiconductor process and device modelling)
   - PVSyst (PV system design)
   - PC1D (solar cells characteristics)

- **Awards**
  - Received best poster presentation award for "Pulsed-DC reactive sputter deposited aluminum oxide for surface passivation of p-type silicon for solar cell applications," at the IIIrd International Conference on Advances in Energy Research (ICAER 2011), held at IIT Bombay

- **Extra- curricular activities**
  - Participated as volunteer for various workshops, conferences and trainings held at IIT Bombay and NISE Gurugram.
  - Active participation in various sports

- **List of publications**

Journal publications

1. **M. Bhaisare**, A. Misra, and A. Kottantharayil, "Aluminum oxide deposited by pulsed-DC reactive sputtering for crystalline silicon surface passivation," *IEEE J. Photovolt.*, vol. 3, no. 3, pp. 930-935, 2013.
2. **M. Bhaisare**, A. Misra, M. Waikar, and A. Kottantharayil, "High quality Al_2O_3 dielectric films deposited by pulsed-DC reactive sputtering technique for high-k applications," *Nanosci. Nanotechnol. Lett.*, vol. 4, no. 6, pp. 645-650, 2012.

Conference publications

3. K. Midya, **M. Bhaisare**, A. Kottantharayil, and S. Dhar, "Investigation of nature of UV induced negative charge in Al_2O_3 film," In Proc. Of 3rd IEEE International Conference on Emerging Electronics, 2016, pp. 1-4.
4. **M. Bhaisare**, S. S. Sandeep, and A. Kottantharayil, "Thermal stability of single layer pulsed-DC reactive sputtered AlOx film and stack of ICP-CVD SiN_x on AlO_x for p-type c-Si surface

passivation," In Proc. Of 2nd IEEE International Conference on Emerging Electronics, 2014, pp. 1-4.

5. **M. Bhaisare**, D. Sutar, A. Misra, and A. Kottantharayil, "Effect of power density on the passivation quality of pulsed-DC reactive sputtered 4rapheme4 oxide on p-type crystalline silicon," In Proc. Of 39th IEEE Photovoltaic Specialists Conference, 2013, pp. 1207-1211.
6. **M. Bhaisare**, G. Jeevanandam, and A. Kottantharayil, "Pulsed-DC reactive sputter deposited aluminum oxide for surface passivation of p-type silicon for solar cell applications," presented at 3rd International Conference on Advances in Energy Research, Mumbai, India, 2011.
7. **M. Bhaisare**, A. Misra, M. Waikar, and A. Kottantharayil, "High quality Al_2O_3 dielectric films deposited by pulsed-DC reactive sputtering technique for high-k applications," presented at International Conference on Materials for Advance Technologies 2011, Singapore, 2011.
8. A. Mishra, H. Kalita, M. Waikar, A. Gour, **M. Bhaisare**, M. Khare, M. Aslam, and A. Kottantharayil, "Multilayer graphene as charge storage layer in floating gate flash memory," *In Proc. of* 4th IEEE International Memory Workshop, Milano, 2012, pp. 1-4.
9. A. Misra, M. Waikar, A. Gour, **M. Bhaisare**, S. Mane, P. Nyaupane, and A. Kottantharayil, "SiO_2/Al_2O_3 dielectric stack with low power pulsed-DC reactive sputtered high-k Al_2O_3 as blocking dielectric for NAND flash application," presented at International Workshop on Physics of Semiconductor Devices 2011, Kanpur, India, 2011.
10. M. A. Khaderbad, R. Pandharipande, A. Gautam, A. Mishra, **M. Bhaisare**, A. Kottantharayil, Y. Meesala, R. Mangalampalli, and V. R. Rao, "Bottom-up Method for Work Function Tuning in High-k/Metal Gate Stacks in Advanced CMOS Technologies," In Proc. of 11th IEEE International Conference on Nanotechnology, Portland, Oregon, 2011, pp. 269-273.
11. A. Misra, S. Sadana, S. Suresh, **M. Bhaisare**, S. Srinivasan, M. Waikar, A. Gaur, and A. Kottantharayil, "Effect of different substrate materials on the Pt nanocrystal formation statistics (size, density area coverage and circularity) for flash memory application," presented at MRS Fall Meeting 2010, Boston, 2010.

Effect of Power Density on the Passivation Quality of Pulsed - DC Reactive Sputtered Aluminum oxide on P - type Crystalline Silicon

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***Abstract* — In this paper we investigate the surface passivation of silicon surfaces by pulsed – DC (p - DC) reactive sputtered Aluminum oxide (AlO_x) films as a function of the deposition power density. The p-DC reactive sputtered AlO_x deposited at power densities of 1.3 W. cm^{-2} and 0.13 W. cm^{-2} showed effective surface recombination velocities (S_{eff}) of 30 cm. s^{-1} and 107 cm.s^{-1} respectively on p - type crystalline silicon surface after a post deposition anneal in a $N_2 + O_2$ ambient at 520 °C. With increase in power density the deposition rate also increases thus improving the throughput. The density of negative fixed charge in the dielectric or the density of interface states, extracted from metal – oxide – semiconductor capacitors, do not show any significant dependence on deposition power. Cross - sectional Transmission electron microscopy shows the presence of thick interfacial layer for these films. X-ray Photoelectron Spectroscopy (XPS) measurements show a significant difference in the stoichiometry of the deposited film as a function of the deposition power.**

***Index Terms* — Aluminum Oxide, Reactive sputtering, Surface passivation, Crystalline silicon solar cells.**

I. Introduction

Aluminum oxide (AlO_x) films synthesized by various techniques have been widely studied for the surface passivation of crystalline silicon (c - Si) solar cells. AlO_x films with effective surface recombination velocity (S_{eff}) < 5 cm. s^{-1} was reported on low resistivity p-type and n-type mono-crystalline wafers by plasma enhanced chemical vapor deposition (PE - CVD) and plasma assisted atomic layer deposition (PA - ALD) techniques [1,2]. The drawback of these techniques is the high cost of the precursors used and the external safety hardware for such precursor. On the other hand for reactive sputtering technique the requirements are only high purity metal target and high purity gases. Zhang et al. [3] reported surface passivation by RF reactive sputtered AlO_x film with S_{eff} ~ 8.5 cm. s^{-1} on n - type Si. It was reported that low power deposition results in better surface passivation. The high quality surface passivation was related to the activation of both field- effect and chemical passivation i.e. high fixed oxide charges (Q_f) in the dielectric and low interface state density (D_{it}). In this work, we have investigated the dependence of the surface passivation quality of pulsed-DC (p - DC) reactive sputtered AlO_x films on the deposition power. The AlO_x films are deposited at different power densities (PD) and their impact on the surface passivation is reported. Contrary to the report on the power dependence in RF sputter deposition, surface passivation property of p-DC reactive sputter deposited films is improving with increasing deposition power. X-ray photoelectron spectroscopy (XPS) indicates that the composition of the deposited film tend to be more stoichiometric with increasing deposition power. Cross-sectional Transmission electron microscopy measurements show the presence of thick interfacial layer for these films, regardless of the deposition power.

II. Experimental Details

AlO_x films were deposited by p-DC reactive sputtering in an Applied Materials PVD Endura system. The detail of the development of deposition process can be found in [4]. The process was carried out at PD between 0.13 and 1.3 W. cm^{-2} with constant pulse frequency of 100 kHz. A high purity Aluminum target (99.9995 %) and Ar and O_2 gases with flow rates of 10 sccm and 55 sccm respectively were used. The base pressure of the system was 7×10^{-8} torr before the deposition. The AlO_x films were deposited on RCA cleaned wafers using the process parameters mentioned above. Metal-oxide semiconductor (MOS) capacitors were fabricated with Al metal gate as front and back contact for investigating the electrical quality on p - type (100) CZ Si wafers of resistivity 5 Ω. cm. For life-time measurements the AlO_x films were deposited on RCA cleaned p- type Si (100) float zone (FZ) wafers of resistivity 7 Ω. cm. AlO_x films are deposited on both sides of the FZ wafers. The films were subjected to post-deposition annealing (PDA) in $N_2 + O_2$ ambient in 79 : 21 ratios to mimic dry air at 520 °C, as this was found to be an optimum anneal condition [5]. The film thickness (t_{ox}) and refractive index (RI) were measured by Sentech spectroscopic ellipsometry (SE 800). Capacitance versus gate voltage (CV) and conductance versus gate voltage (GV) of the MOS capacitors were measured at a frequency of 100 kHz using a Keithley 4200 semiconductor characterization system. The

Aluminum Oxide Deposited by Pulsed-DC Reactive Sputtering for Crystalline Silicon Surface Passivation

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***Abstract*—In this paper, we report on the surface passivation of crystalline silicon (c-Si) by pulsed-dc (p-dc) reactive-sputtered aluminum oxide (AlO_x) films. For the activation of surface passivation, the films were subjected to post deposition annealing (PDA) in different ambients namely N_2, $N_2 + O_2$, and forming gas (FG) in the temperature range of 420–520 °C. The surface passivation was quantified by surface recombination velocity, which was correlated to the interface states at the silicon–dielectric interface and fixed charges in the dielectric. A good quality surface passivation with effective surface recombination velocity $S_{\rm eff}$ of 41 $\rm cm \cdot s^{-1}$ is obtained for PDA in N_2 or $N_2 + O_2$ gas ambient. PDA in FG ambient at high temperature is found to degrade the passivation. The AlO_x film annealed in FG ambient shows poorer thermal stability as compared with films annealed in the other two ambients. A clear path for further improvements in surface passivation quality of p-dc reactive sputter-deposited AlO_x is suggested based on cross-sectional transmission electron microscopy and X-ray photoelectron spectroscopy analysis and electrical data.**

***Index Terms*—Aluminum oxide, crystalline-silicon solar cells, pulsed-dc reactive sputtering, surface passivation.**

I. Introduction

ALUMINUM OXIDE (AlO_x) films are widely investigated for surface passivation of crystalline-silicon (c-Si) solar cells [1]–[3]. For AlO_x deposition, atomic-layer deposition (ALD; thermal and plasma assisted) [4]–[12], and plasma-enhanced chemical vapor deposition (PECVD) [8], [13] are the most widely studied techniques. The effective surface recombination velocities $S_{\rm eff} < 10$ $\rm cm \cdot s^{-1}$ are reported using either technique on both p-type and n-type c-Si surfaces. To activate the passivation, the films are subjected to a post deposition anneal (PDA), which results in the enhancement of negative fixed-oxide charge Q_f in the dielectric and reduction of the interface state density D_{it}, hence improving both field-effect and chemical passivation, respectively. The PDA has been performed in N_2 [4], [5], [7], [8], forming gas (FG) [11], [14] or air [9] ambients with temperatures in the range of 300–550 °C. The AlO_x films deposited by ALD and PECVD techniques contain 2–7% hydrogen [8]. It is also reported that an interfacial silicon oxide (SiO_x) of thickness 1.5–2 nm is formed between the AlO_x and the silicon surface during the ALD processes [1], [4]. The improvement in passivation quality after PDA is also related to the diffusion of hydrogen from the AlO_x film to the Si–SiO_x interface during the annealing process [7], leading to chemical passivation of the interface [7], [15]. However, effusion of hydrogen from the AlO_x film at higher temperatures (typical temperature used in contact firing for screen printed solar-cell process), results in the degradation of passivation [7]. Blistering of AlO_x films deposited by ALD and PECVD techniques, with and without a silicon nitride capping layer, is reported upon high-temperature firing and is attributed to the release of large amounts of H_2 from the film [16], [17]. Even though the passivation quality was not seen to degrade as a result of blistering, it is expected to cause shunting in solar cells [17]. As a consequence, the deposition process should be carefully controlled to avoid large amounts of hydrogen in the film or to restrict the effusion of the hydrogen.

The sputter-deposition technique offers several advantages, like 1) significantly low-consumable cost since only aluminum metal, argon, and oxygen gases are required; 2) sputtering process can be carried out at room temperature, whereas ALD or PECVD process at room temperature results in high carbon content in the film; and 3) the deposited film is unlikely to contain large amounts of hydrogen as the starting materials do not contain hydrogen. This could solve some of the issues related to high hydrogen concentration as seen in ALD and PECVD films. However, hydrogen can be introduced into the film during post deposition process and hence the film deposited by the sputtering process could be used as a test vehicle to study the role of hydrogen in surface passivation.

Li and Cuevas [19] reported $S_{\rm eff}$ of 16 $\rm cm \cdot s^{-1}$ and 14 $\rm cm \cdot s^{-1}$ for radio frequency (RF)-sputtered AlO_x films after PDA in N_2 and FG ambients, respectively, at 400 °C. The RF-sputtered AlO_x films result in mid-gap interface states densities D_{it} of 4×10^{12} $\rm cm^{-2} \cdot eV^{-1}$ and negative fixed oxide charge density Q_f of 3×10^{12} $\rm cm^{-2}$ after PDA in N_2 at 500 °C [19]. Schmidt *et al*. [20] demonstrated p-Si passivated emitter and rear cell (PERC) solar cells with RF-sputtered AlO_x for rear-surface passivation, and open-circuit voltage $V_{\rm OC}$ values of 651 mV was reported with $S_{\rm eff}$ in the range of 35–70 $\rm cm \cdot s^{-1}$. Krugel *et al*. [3] demonstrated a stack of reactive-sputtered AlO_x/SiN_x films for rear-surface passivation of p-type "laser fired contacts (LFC)-PERC" solar cells with efficiency η of 18.5%, and shows an improvement of 0.8% over the back surface field (BSF) reference cells. Zhang *et al*. [18] demonstrated that a significantly lower $S_{\rm eff}$ of 8 $\rm cm \cdot s^{-1}$ could be obtained by optimizing the

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High Quality Al_2O_3 Dielectric Films Deposited by Pulsed-DC Reactive Sputtering Technique for High-k Applications

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This paper presents high quality high-k Al_2O_3 dielectric films deposited by reactive sputtering technique with pulsed-DC (p-DC) power supply source. Process parameters are optimized to obtain Al_2O_3 dielectric film with high effective breakdown field (E_{BD}) of 18.07 MV/cm and dielectric constant (k) of 8.15 with an equivalent oxide thickness (EOT) of 8.59 nm, suitable for inter-poly dielectric (IPD) of floating gate flash memory applications. X-ray photoelectron spectroscopy (XPS) measurement is performed for films deposited with different gas flow ratios and it is observed that the film stoichiometry can be changed by varying the gas flow ratio. A low surface roughness of 3.2 Å is observed by atomic force microscopy (AFM) measurement on these films. Al_2O_3 films deposited at high power are found to be interesting for surface passivation of *p*-type silicon for solar cell applications.

Keywords: High-k Al_2O_3 Dielectric, Inter-Poly Dielectric (IPD), Reactive Sputtering, Pulse-DC Power Supply, Surface Passivation for Silicon Solar Cell.

1. INTRODUCTION

High-k Al_2O_3 is being extensively investigated for various applications like gate oxide for scaled CMOS transistors,[1] tunnel oxide and IPD for flash memories[2] and surface passivation in solar cells.[3] The reactive sputtering is an attractive option as the resultant film would be free of organic and other contaminants, which could be a problem in chemical vapour deposition (CVD) processes.[4, 5] Also CVD technique requires expensive precursors which are generally hazardous and thus also needs expensive safety equipments. The cost of deposited films can be reduced significantly using p-DC reactive sputtering technique because it requires only the metal, the reactive gas (O_2) and the sputtering gas (Ar). p-DC does not require an impedance matching network unlike an RF sputtering process. However the sputter deposited films have historically shown poor electrical characteristics as compared to CVD films due to sputter damage and low density.[6, 7]

In this paper we present an optimized process for p-DC reactive sputtered high-k Al_2O_3 film with high E_{BD} of 18.07 MV/cm and low leakage current density (J_G)3×10^{-9} A/cm^2 measured at gate voltage (V_G) of −5 V with EOT 8.59 nm, which is a potential choice for the IPD of floating gate NAND flash memory.[8–12] Also in the later part we have demonstrated that the high power deposited Al_2O_3 film gives high density of negative fixed oxide charges (Q_{ox}) in the order of 2.88×10^{12} cm^{-2} that is suitable for surface passivation of *p*-type silicon surface for solar cell application.[3, 13–15] The paper is organized as follows: experimental details are outlined in Section 2, the results of material and electrical measurements are presented and discussed in Section 3, and conclusions are drawn in Section 3.

2. EXPERIMENTAL DETAILS

The Al_xO_y dielectric film was deposited on 4" *p*-type Si (100) wafers in PVD chamber of Applied Materials ENDURA cluster tool. A schematic of the sputter system is shown in Figure 1(a). Al_2O_3 film is deposited by reactive sputtering of high purity aluminum target (99.9995% pure) with O_2 as a reactive gas and Ar as sputtering gas, which generates heavy Ar^+ ions to remove atoms from the target surface. The Al target is connected to cathode where a p-DC supplies continuous negative/positive pulses (V_P) (Fig. 1(b)), while the substrate is connected to anode

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PULSED–DC REACTIVE SPUTTER DEPOSITED ALUMINUM OXIDE FOR SURFACE PASSIVATION OF P-TYPE SILICON FOR SOLAR CELL APPLICATIONS

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Abstract

In this paper we have investigated the surface passivation of p-type silicon using aluminum oxide deposited by pulsed-DC reactive sputtering. A deposition rate of 5-7 nm/min is obtained using this technique, and this is significantly higher than typical ALD processes investigated for solar cell passivation. Properties of films processed under different deposition power were investigated using XRR and ellipsometry. Deposition rate and refractive index were found to increase with power. The films were found to contain high density of negative fixed charges, and the charge density increased with deposition power. After FGA annealing, the negative fixed charge density increased to 7 X 10^{12} cm^{-2}. As a consequence the surface recombination velocity was seen to improve by one order of magnitude to 1000 cm/sec. FGA annealing however is not effective in reducing the interface trap density.

Keywords: Aluminum Oxide, Pulsed- DC reactive sputtering, Surface passivation, Silicon Solar cell

1. Introduction

The AlO_X dielectric has been widely investigated for surface passivation of p-type silicon. The mechanism of surface passivation is mainly due to the repulsion of electrons from the surface of Si by the negative charges in the dielectric (Hoex et al. 2006a, 2007b, 2008c). High density of negative charges in the range of 10^{12} to 10^{13} cm^{-2} are reported for AlO_X/p-Si system when the dielectric is deposited by ALD, PE-ALD and PE-CVD techniques. Dingemans and Kessels et al.(2010a 2010b) noted that a low interface state density in the range of 10^{11} $eV^{-1}cm^{-2}$ is also desirable for achieving high quality passivation. Various deposition techniques for AlO_X deposition including ALD, PECVD and RF reactive sputtering were reported by Schmidt et al. (2010). Even though ALD films provided the best passivation with an effective surface recombination velocity (S_{eff}) of 6 cm/s, sputter deposited films resulted in S_{eff} of 55 cm/s. PERC cells incorporating these films for rear side passivation gave V_{OC} of 662 and 651 mV respectively with corresponding efficiencies of 21.4 % and 20.1 %. ALD is a slow process with a low deposition rate and requires expensive precursors (Dingemans, 2010a). Sputtering on the other hand could be fast and requires only an Al target, and O_2 and Ar for deposition of AlO_X. Pulsed-DC sputtering could be more attractive than an RF system as no RF matching networks and associated hardware are required in the former.

In this work we present a reactive sputtering technique using pulsed-DC power supply for AlO_X deposition and present a preliminary analysis of the potential of the film for surface passivation of p-type silicon. The reactive sputtering of pure Al target (99.9995% purity) is carried out in high purity oxygen ambient with argon as sputtering gas. It was reported by Kelly et al. (2000) and Jonsson et al. (2000), that by using pulsed-DC power supply continuous dielectric sputtering is possible with an arc free environment. During the positive part of pulse, electrons are attracted to the surface and neutralize the positive charges which builds-up on the surface of the target and chamber walls during sputtering (i. e. negative voltage). The AlO_X is deposited on p-type silicon wafer for investigation of various process and material characteristics like deposition rate and refractive index (by spectroscopic ellipsometry), and density and surface roughness (by X-ray reflectivity). The films and their interface with p-type silicon were subsequently characterized using high frequency capacitance – voltage (CV) characteristics of metal oxide semiconductor (MOS) capacitors. Effective surface recombination velocity is calculated from minority carrier life-time measured by the quasi-steady state photo-conductance (QSSPC)

High Quality Al2O3 Dielectric Films Deposited by Pulsed DC Reactive Sputtering Technique for High-k Applications

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This paper represents reactive sputtering technique with pulsed-DC power supply source for deposition of high quality high-k Al_2O_3 dielectric films. In this technique the quality of deposited film depends on various parameters like gas flow ratio (i.e. partial pressure), applied power and substrate temperature during deposition. Reactive sputtering is an attractive option as the resultant film would be free of organic and other contaminants, which could be a problem in CVD processes. The hysteresis behavior is observed in cathode voltage because only after a certain value of O_2 flow the metal target surface is oxidized and become a metal-oxide, which causes a sudden drop in cathode voltage and during the retrace the target voltage rises to its initial value. From the XPS measurement the stoichiometric Al_2O_3 film is obtained at O_2 flow slightly above knee point on the hysteresis curve, while the film become O rich for higher O_2 flow. The deposition rate decreases with increasing O_2 flow, due to an increase in the process pressure that cause a decrease in mean free path and hence the sputtering rate. A low surface roughness of 3.2 Å is observed by AFM measurements on films deposited with Ar: O_2 flow ratio of 1:2.5. The effective breakdown field of 18.07 MV/cm is obtained by our optimized process and is comparable to values reported for films deposited by CVD Al_2O_3 [1]

Conclusion

In this paper we have demonstrate higher effective breakdown field of 18.07 MV/cm for reactive sputtered high-k Al_2O_3 film and a dielectric constant of 8.15 is achieved. Through XPS analysis it is demonstrated that the stoichiometric film is obtained at O_2 flow slightly above the knee point of forward path in the hysteresis curve.

References [1] Y.Y Chen et al., Proc. IEEE Conf. Emerging Technologies-Nanoelectronics, (2006), 463

Multilayer Graphene as Charge Storage Layer in Floating Gate Flash Memory

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Abstract— Charge storage capability of multilayer graphene (MLG) in floating gate flash memory structure is demonstrated. MLG sheets are considered for this purpose because of the higher work function and higher density of states compared to single layer graphene (SLG) and lower conductivity along c-axis. A memory window of 6.8V for 1 second programming is obtained at ±18V program/erase voltage. Number of electrons stored in MLG sheets after 18V programming voltage is calculated as 9.1 x 10^{12} cm^{-2} which is higher than the density of states in SLG, suggesting the suitability of MLG for multi level data storage flash memory devices.

Keywords-component; formatting; Flash Memory, Multilayer Graphene, Program Erase Transisent

I. INTRODUCTION

LATERAL and vertical scaling of flash memory devices lead to high data storage capacity and low program/erase voltages for these devices. However, lateral scaling also results in increased capacitive coupling between the floating gates of adjacent cells [1]. The parasitic capacitive coupling between neighboring cells causes a wide distribution in threshold voltages of the devices [1]. Floating gate height reduction is one possible way to reduce the capacitive coupling [1]. Recently it has been demonstrated that conventional polycrystalline silicon (poly-Si) floating gate thickness can be reduced to 7nm [2]. However, a significant fraction of electrons injected into such thin poly-Si would be ballistically transported through the floating gate, and this would result in slower programming [2]. These ballistic carriers may also cause impact ionization in the blocking dielectric and thus degrade the dielectric reliability. To alleviate these issues with thin poly-Si floating gate, use of a thin metal layer in place of thin poly-Si is proposed and a 1nm thick metal layer as a floating gate material is found to be capable of suppressing the ballistic current component [2,3]. Metal floating gate, however, may impose its own device variability and reliability issues at high temperatures such as: (i) agglomeration of thin metal layers [4], (ii) diffusion of metal into the tunnel and blocking dielectrics [5], and (iii) increased leakage current through the blocking dielectric deposited on metal films due to higher degree of dielectric crystallization at elevated temperatures [6].

Since graphene is the thinnest naturally stable sheet having metallic properties, it would be interesting to use graphene in place of poly-Si or metal as a charge storage layer in floating gate flash memory. Since the interlayer spacing between two graphene sheets in MLG is only 0.34nm, 6-7 layers of MLG sheets would be 2 - 3 nm thick. Therefore, incorporation of MLGs as floating gate layer in flash memory structure may lead to substantial reduction in the vertical dimension of these devices. Graphene is reported to be thermally stable upto 1500°C [7], and hence thermal stability issues anticipated with metal floating gate may not be a problem with graphene.

Previously, nonvolatile memories (NVM) based on graphene [8-11] and graphene oxide (GO) [12] have been reported. In most of these reports, with the exception of [11] and [12], the device structure and memory operation is different from the existing floating gate flash technology. In [11], a hysteresis of 6V in capacitance – voltage (CV) characteristics of floating gate metal-oxide-semiconductor (MOS) capacitors incorporating graphene is reported when the gate voltage is swept from -7V to +7V and back. However the authors noted that the gate leakage at -10V is negligibly small (7 x 10^{-7} A/cm^2), presumably due to the thick dielectric stack (5nm SiO_2 and 35 nm Al_2O_3) used. Based on this data, mechanism behind such low voltage programming with the reported gate stack is ambiguous. While in [12], a hysteresis of 7.5V for ±14V voltage sweep in the C-V curve is reported with MOS capacitors incorporating GO as floating gate. However, thermal instability of the GO due to the presence of oxygen functional groups [13] is a serious concern for silicon based devices, where high temperatures in the range of 1000°C are used for processing. In [12], charge storage capability of reduced single layer GO is also demonstrated with a memory window of 1.4V.

We have investigated charge storage capability multilayer graphene (MLG) sheets. MLG is chosen for several technical advantages over their single layer analogs. SLG has a work function (WF) of 4.2 eV. WF of MLG is susceptible to the number of layers, when it is less than 4. For thicker MLG sheets (> 4 layers) WF saturates to a value of 4.6eV [14]. Accurate control of the number of sheets on large areas

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SiO_2/Al_2O_3 dielectric stack with low power pulsed-DC reactive sputtered High-K Al_2O_3 as blocking dielectric for NAND flash application.

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***Abstract*—The Dielectric stack containing SiO_2 as tunnel dielectric and Al_2O_3 as blocking dielectric is widely explored for NAND Flash Memory application. Here we have studied the electrical properties such as breakdown field, dielectric constant (K), interface trap density (D_{it}) etc. of the dielectric stack containing high quality thermally grown SiO_2 as tunnel dielectric and low power pulsed-DC reactive sputtered Al_2O_3 as blocking dielectric for NAND flash memory application. Al_2O_3 deposition rate, refractive index, bulk oxide charges, D_{it} and K as a function of different low power depositions are studied. Stoichiometry of the Al_2O_3 film for different process conditions is analyzed by X-ray photoelectron spectroscopy (XPS) data.**

***Index Terms*— NAND Flash, tunnel and blocking dielectric, low power pulsed-DC.**

I. INTRODUCTION

For NAND Flash memory application high quality thermally grown SiO_2 is used as the tunnel dielectric due to excellent interface it forms with the silicon substrate with less interface traps and thus is reliable to achieve long term data retention. The pulsed DC reactive sputtered High-K Al_2O_3 could be an interesting candidate as high dielectric constant blocking dielectric in flash memory because it is free of organic and other contaminants as compared to films deposited by CVD or ALD. RF sputtering, though being a choice for reactive sputtering of dielectrics, is costly, has low deposition rates and its reliability issues reduces its chances of acceptance in high volume production [1].The sputter induced damage is the main concern for reactive sputtered Al_2O_3 film. We have tried to address this issue by studying the electrical parameters of the blocking dielectric by low power deposition experiments and selecting the optimum power. Depositions were carried out at 150W, 200W, 300W and 400W aluminum target powers and it was found that depositions done at 200W power for Al_2O_3 gives optimum results in terms of refractive index, dielectric constant, stoichiometry of film. Less negative oxide charge and higher breakdown field are obtained for 200 W deposition compared to other cases.

II. EXPERIMENTAL DETAILS

Si/SiO_2- Al_2O_3/Al MOS capacitors were used as the test structure for the investigations reported below. 4" Si (100) wafers were cleaned by standard RCA cleaning process. High quality SiO_2 is grown on the wafers by thermal oxidation at 800^0C for 5min in a horizontal hot wall furnace to obtain 3.2nm SiO_2. Al_2O_3 dielectric film was subsequently deposited on SiO_2 in PVD chamber of Applied Materials (AMAT) ENDURA cluster tool by pulsed-DC reactive sputtering of an aluminum target with Ar as sputtering gas and O_2 as the reactive gas at target powers of 150W, 200W, 300W and 400W at chamber pressure of 1.33 mTorr. The gas flow ratio Ar:O_2 was 10:(knee point+5) where knee point as well as target voltage to be maintained to achieve target conditioning is obtained from hysteresis curve as shown in Fig. 1 [2]. The samples were annealed under various conditions after Al_2O_3 deposition to densify the Al_2O_3 films. Aluminum was evaporated on top of the Al_2O_3 and patterned using optical lithography and reactive ion etching to obtain capacitors with circularly shaped gates having diameter of 80µm. Deposited films were characterized by ellipsometry, XPS and the MOS capacitors were subjected to FGA anneal at 420^0C for 20 minutes and characterized by current-voltage and capacitance-voltage measurements.

III. RESULTS AND DISCUSSIONS

The high frequency CV curves for dielectric stacks were obtained for different Al_2O_3 deposition powers as shown in Fig. 2. For deposition done at 200W, Q_{OX}=8 x $10^{11}cm^{-2}$ and D_{it}=6 x $10^{11}cm^{-2}eV^{-1}$, which are less than for higher power deposition, Fig. 3. From the J-E plots of the MOS capacitor, Fig. 4, the breakdown field of the film deposited at 200 W power is seen to be the highest. The deposition rate (1.14nm/min) and RI (1.54) of film deposited at 200W are as shown in Fig 5. The film deposited at 150 W has much lower RI, suggesting that the film could be less dense. On the other hand, deposition at higher power than 200 W is seen to result in sputter damage. The film deposited at 200W was further studied by annealing the Al_2O_3 after deposition at 700^0C, 800^0C and 900^0C for 15 sec in O_2 ambient. From the CV (Fig. 6) and the extracted D_{it} (fig. 7), it is seen that the dielectric constant increases and the interface state quality improves with annealing. 200W deposition and anneal at 900^0C gives high effective breakdown field of 16.2 MV/cm (Fig. 8), lowest D_{it}=2 x $10^{12}cm^{-2}eV^{-1}$ (Fig. 7) and the highest K =7.53 (Fig. 7) when compared to films annealed at 700^0C and 800^0C. Using XPS analysis the O 1s spectra and Al 2p spectra were generated and compared for unannealed and 900^0C annealed, 200W deposited films as shown in fig. 10 (a) & (b). The ratio O_2:Al extracted from XPS data was 2.1 and 1.75 for unannealed and 900^0C annealed films respectively, the later being closer to the stoichiometric ratio of 1.5.

IV. CONCLUSIONS

In conclusion, the low power (200W), 900^0C annealed pulsed-DC reactive sputtered Al_2O_3 seems to be good option for blocking dielectric in flash application as it has good breakdown field, RI, dielectric constant, less D_{it} and negative oxide charges, good Stoichiometry.

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Bottom-up Method for Work Function Tuning in High-k/Metal Gate Stacks in Advanced CMOS Technologies

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Abstract—**In this paper we have studied the application of porphyrin self-assembled monolayers (SAMs) for metal-gate work function tuning in high-k/metal gate technologies. Varying the dipole moment in porphyrin macrocycles by changing its central metal ion has been used to modify the work function. For HFCV analysis, porphyrin SAM was prepared on MOCVD grown hafnium oxide (HfO_2) and on sputtered aluminum oxide (Al_2O_3) gate oxides followed by Al evaporation to form MOS capacitors. UV absorption and FTIR spectra show the formation of SAM on high-k while the thermal gravimetric analysis (TGA) on Zn-porphyrin shows that the molecule is stable upto 450^{0}C and can be effectively implemented in high-k/metal gate technologies involving gate-last CMOS processes.**

Index Terms – work function tuning, porphyrin, high-k, dipole, self assembled monolayer

I. Introduction

Over the last four decades, feature sizes in complementary metal oxide semiconductor (CMOS) technologies have been scaled from 3 μm to the current sub-32 nm using the "top-down" scaling techniques [1]. Now, conventional scaling involving polysilicon–SiO_2 has to be replaced because of the short-channel effects (SCEs) such as direct gate tunneling leakage current, poly depletion and boron penetration [2]. To overcome the above fundamental problems, high dielectric constant (high-k) gate oxides and metal gate electrodes are being researched upon. After a decade of research involving an exhaustive search for new gate dielectric materials and metal gate electrodes, the first commercial use of high-k gate dielectrics and metal gate electrodes has been demonstrated by Intel in its 45nm node CMOS technology. After the 45nm process technology's success, industry is now moving towards second generation high-k+metal-gate technologies at the 32nm node [3].

High-k dielectrics, such as Al_2O_3, CeO_2, Y_2O_3, HfO_2, La_2O_3 and ZrO_2 are looked upon as potential candidates for gate dielectric applications [4-6]. Among them, Hafnium based high-k materials are the primary candidates that have replaced the silicon oxynitride gate dielectric as they have promising characteristics such as low leakage current, good interface properties, good thermal/chemical stability and sufficient band offsets to Si [7, 8]. Though, Al_2O_3 has a lower permittivity, its larger band gap makes it a good barrier layer in stacked structures [9].

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The major advantage of the traditional poly-Si gate electrode is the ability to make a Fermi-level adjustment by either donor or acceptor implantation. With aggressive scaling, sheet resistance associated with the polysilicon gate, poly depletion and threshold voltage (V_t) fluctuations due to boron penetration into the gate oxides are becoming major issues in device/circuit performance [10]. Moreover, Fermi-level pinning causes V_t instabilities and other reliability issues [11]. Consequently, mid-gap metals and dual work function metals are required to be integrated to eliminate above problems. Appropriate metal gates have requirements which include good thermal/chemical interface stability with underlying dielectric and should have an appropriate work function for NMOS or PMOS devices (~4eV for NMOS and ~5eV for PMOS). Using mid-gap metal for PMOS and NMOS may lead to high threshold voltages, where as the use of two different metals for PMOS and NMOS devices requires complicated processing steps. This makes metal-gate work function tuning very important for the current and future CMOS technologies.

To meet the above explained requirements, transition metals such as W, Ti, Ta, Mo, Ru and their metallic derivatives, WN, TiN, TaN, MoN, TaSiN, and MoSiN are used as metal gates. These transition metals are known to possess some desirable properties such as mid-gap work function, high melting point, low resistivity and thermal stability at high temperatures. The work function tuning of the above gates has been successfully implemented using various techniques including alloying, metal inter-diffusion, dopant implantation, silicidation and nitridation [12-14]. A viable alternate solution is the use of SAM of organic molecules, between a metal and a gate dielectric, to tune the work function of the metal gate.

With the derivatives of alkanethiols SAMs, it was demonstrated that the work function of Ag (Φ_{Ag} ~4.4 eV) can be increased to 5.5 eV ($\Delta\Phi$ ~ 1.1 eV). The ordering of molecules in SAMs creates an effective dipole at the metal/SAM, which enables the change in metal work function [15, 16]. Such a technique was implemented and used for the manipulation of charge injection in OFETs. Recently, spatial tuning of the metal work function was realized with the surface-chemical gradients composed of SAMs of decanethiol (DT) and a partially fluorinated decanethiol (PFDT) on gold, prepared by controlled-immersion process. In that work, the work function of SAM covered gold, compared to the work function of pure gold (Φ_0), was lowered ($\Delta\Phi < 0$) upon DT adsorption, whereas it was raised ($\Delta\Phi > 0$) upon PFDT adsorption [17]. Porphyrins and their derivatives show barrier properties on various metals [18]. Potential use of these multi-functional

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Effect of Different High-K Dielectrics on the Pt Nanocrystal Formation Statistics (size, density and area coverage) for Flash Memory Application

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ABSTRACT

We here present, metal nanocrystal (NC) formation statistics (size, density, occupancy or area coverage) on different high dielectric constant (high-K) materials which may be used as tunnel dielectric or intermetal dielectric in flash memory devices. Four important high-K materials *viz.* SiO_2, Al_2O_3, HfO_2 and Si_3N_4 are chosen for this purpose and the nanocrystal formation statistics has been found to be strongly dependent on dielectric. Among all the four dielectrics, smallest size nanocrystals with largest density are obtained on Al_2O_3 dielectric while on HfO_2 bigger size nanocrystals are formed. This difference in nanocrystal size and density on different dielectrics is attributed to the different surface properties of these materials.

INTRODUCTION

Metal nanocrystal (NC) based NAND flash memories, proposed by Liu *et.al* [1], are being investigated for sub -22 nm node flash devices. Metals have the benefits of availability of different work functions which provides the freedom to tailor the programming/erasing and retention characteristics of the memory devices. To enable the continuous scaling of the overall flash gate stack, the use of high-K materials as tunnel dielectric in place of conventional SiO_2 is also being proposed. In that case nanocrystal formation would occur on high-K dielectric and not on the SiO_2 layer. Apart from this, dual layer nanocrystal memories are also studied to increase the memory window of the flash devices [2]. In this case again, the nanocrystal formation for the second layer is most likely would be on some high-K material which may be different from the bottom tunnel dielectric. Both the dielectrics will have different surface energies and different roughness, leading to the variation in NC size and density. Since NC flash memory performance strongly depends on the NC size, density, and occupancy, hence it is inevitable to study the nanocrystal formation statistics on different high-K materials which may be used as tunnel oxide or as an intermetal dielectric (in case of dual layer devices) in flash devices.

The procedures available for the nanocrystal formation include colloidal, aerosol, and self assembly methods [3]. The limitation of the colloidal process is the contaminations associated with the chemical solution used for the precipitation of the NCs and hence it is not CMOS compatible. In aerosol method, NCs are formed in the gas phase condensation and fall on the substrate. Particle delivery and non uniformity in the sizes of the NCs is a concern with this method. Self assembly method is the easiest and most commonly used method for the NC formation because of its compatibility with standard CMOS process flow. In this method, a very thin metal film is deposited on the tunnel dielectric and is subsequently annealed at suitable