Poonam Jayal

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DOB: July 26, 1982
Marital status: Married
Maiden Name: Poonam Nautiyal
Languages Known: English, Hindi
Place of origin: Uttarakhand, INDIA

MOTIVATION

Looking for an academic role to foster my teaching passion by imparting quality education to budding engineers whole-heartedly cooperating in their quest for knowledge and overall development to the best of my abilities.

PROFESSIONAL HISTORY

ASSISTANT PROFESSOR **2011 – 2015**
Bharati Vidyapeeth's College of Engineering New Delhi, INDIA

Teaching and mentoring the undergraduate students of Electrical Engineering, conducting laboratory and theoretical classes. Evaluating their performance based on continuous assessments and project works. Organizing workshops, guest lectures, industrial tours etc. for students & faculty. Initiated a student chapter of International Society of Automation (ISA-BVP) in the institute.

SENIOR LECTURER **2008 – 2009**
G.L Bajaj Institute of Technology and Management, NCR Delhi, INDIA

Teaching the undergraduate students of Electrical Engineering, actively involved in industry-academia liasioning being the training and placement faculty representative of the Electrical Engineering department.

ADHOC LECTURER **2004 – 2007**
Goa College of Engineering, Ponda, Goa, INDIA

Teaching the undergraduate Electrical Engineering students, conducting laboratory and theoretical classes, and evaluating them based on continuous assessments.

GRADUATE TRAINEE **2003 – 2004**
Mormugao Port Trust, Vasco-Da-Gama, Goa, INDIA

ACADEMIC PROFILE

PhD, Power Electronics, Electrical Machines and Drives
IIT Delhi, Delhi, INDIA **2015 – 2020**

Master of Engineering, Control & Instrumentation
Delhi College of Engineering (Present DTU), Delhi, INDIA **2009 – 2011**

Bachelor of Engineering, Electrical Engineering
Goa College of Engineering, Goa, INDIA **1999 – 2003**

Senior Secondary School
Kendriya Vidyalaya - 1, Vasco Da Gama, Goa, INDIA **1998-1999**

Higher Secondary School
Kendriya Vidyalaya - 1, Vasco Da Gama, Goa, INDIA **1996-1997**

TECHNICAL COMPETENCIES

- ✓ Knowledge of experimental implementation of power converters using DSPs (F28377s, F28379D).
- ✓ Proficiency in MATLAB/Simulink for Power electronics and electrical machines-based simulation and analyses.
- ✓ Experience in performing experiments with electrical machines and inverter modules incorporating all related laboratory equipments like DSOs, voltage and current probes, power analyzers etc.

ACHIEVEMENTS

- ✓ Second rank in Master of Engineering in the batch of 2009 in Control & Instrumentation at Delhi College of Engineering.
- ✓ University topper in Electrical Engineering (Bachelor of Engineering) in the batch of 1999 at Goa University.
- ✓ Second rank in Tenth grade (C.B.S.E Board) in the batch of 2007.
- ✓ Initiated a student chapter of International Society of Automation (ISA-BVP) at Bharati Vidyapeeth's college of Engineering in September 2014.
- ✓ Organized several workshops, guest lectures, industrial tours etc. for students & faculty, in my teaching career so far

COURSES TAUGHT SO FAR

- ✓ Basic Electrical Engineering
- ✓ Electrical Machines
- ✓ Op-Amps and Linear Integrated Circuits
- ✓ Network and Circuit Analysis
- ✓ Microprocessors and Microcontrollers
- ✓ Process Control
- ✓ Control System
- ✓ Laboratory classes of the above

Poonam Jayal

Ph.D. RESEARCH TOPIC

Performance Analysis and Control of a Reduced Switch Multilevel Inverter Fed Permanent Magnet Synchronous Motor Drive.

RESEARCH SUMMARY

Multilevel inverters (MLIs) with reduced number of switches ensuring cost optimisation are being increasingly sought after for motor drive applications. Also, the design of an appropriate modulation scheme, especially space vector modulation (SVM) scheme, which is one of the most desirable firing methods for MLIs, is indispensable for newer topologies. My research work explores a reduced switch five-level MLI topology (Transistor – Clamped H Bridge inverter) and explores its implementation for the closed loop control of a PMSM drive for Electric vehicle (EV) applications. A generalized SVM scheme is also proposed for any (2^n+1)-level inverter and thereafter proposed as a novel modulation scheme for the five-level reduced switch inverter topology.

RESEARCH PUBLICATIONS

(JOURNALS)

[1] "Reduced Switching Analysis-Based Space Vector Modulation Algorithm for Multilevel Inverters," in *International Journal of Power and Energy Systems*, vol. 39, no. 2, pp.64-76, Nov 2019. (DOI : 10.2316/J.2019.203-0156)

[2] "A Novel Space Vector Modulation-based Transistor-Clamped H Bridge Inverter-Fed Permanent Magnet Synchronous Motor Drive for Electric Vehicle Applications" in *International Transactions on Electrical Energy Systems (Wiley),* vol. 31, no. 3, e12789, March 2021. (DOI: 10.1002/2050-7038.12789)

(INTERNATIONAL CONFERENCES)

[1] "Space Vector Based Enhanced Modulation Scheme for a Reduced Switch Five-Level Inverter," *2020 IEEE 9th Power India International Conference (PIICON)*, SONEPAT, India, 2020, pp. 1-6.

[2] "Simplified Sensor Based Vector Control of Permanent Magnet Synchronous Motor Drive," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, Cochin, India, 2020, pp. 1-6.

[3] "Vector control of permanent magnet synchronous motor drive using a reduced switch five-level inverter," *2018 IEEMA Engineer Infinite Conference (eTechNxT)*, New Delhi, 2018, pp. 1-6.

[4] "Performance analysis and control of permanent magnet synchronous motor drive over a wide speed range," *2017 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC*), Bangalore, 2017, pp. 1-5.

REFERENCES

1) Prof. (Dr.) G. Bhuvaneswari, IIT Delhi (Ph.D. Supervisor)
   http://ee.iitd.ernet.in/people/gbhuv.html
   https://www.mahindraecolecentrale.edu.in/faculty/bhuvaneswari-gurumoorthy
2) Prof. (Dr.) Anandarup Das, IIT Delhi (Student Research Committee Expert)
   https://ee.iitd.ac.in/people/anandarup.html
3) Prof. (Dr.) Prof. (Dr.) Madhusudan Singh, DTU (M.E supervisor)
   http://www.dtu.ac.in/Web/Departments/Electrical/faculty/madhusudan.php
4) Prof. (Dr.) Rajeev Agarwal (Director, G.L Bajaj Institute of Technology and Management)
   https://www.glbitm.org/about_us.aspx?mpgid=2&pgid1=6&pgidtrail=9
5) Prof. (Dr.) Anant J Naik (Faculty at Goa College of Engineering)
   http://www.gec.ac.in/Employe_ProfileNew.aspx?nDeptID=1222&PageId=1

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RESEARCH ARTICLE

WILEY

A novel space vector modulation-based transistor-clamped H bridge inverter-fed permanent magnet synchronous motor drive for electric vehicle applications

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Summary

Electric vehicles (EVs) require an extremely efficient power train unit consisting of converters with very low power losses and a motor with excellent controllability, long life, and an extended speed range. Consequently, permanent magnet synchronous motor (PMSM) drives are increasingly becoming popular for EV applications due to their higher torque density, better efficiency, and rugged structure. This paper explores the reduced switch five-level transistor—clamped H bridge (TCHB) inverter topology for driving a PMSM, particularly for an EV application. The TCHB inverter emulates the modular structure of a cascaded H bridge (CHB) inverter, with each phase being energized by independent DC sources, thereby making it a natural fit for EVs. Simplified loss models have been developed to estimate the conduction and switching losses in the TCHB and CHB inverter circuits to assess their suitability for EV applications. An experimental prototype of the TCHB inverter, triggered with a novel space vector-based modulation scheme, feeding a vector-controlled PMSM has been designed, developed, and tested to ascertain the efficacy of this inverter-motor electrical drive system for light-duty EV applications, with regard to reduced losses, better DC bus utilization, diminished torque ripples, and improved dynamic response.

KEYWORDS

electric vehicles, loss model, multilevel inverters, PMSM, SVM

List of Symbols and Abbreviations: CHB, Cascaded H bridge; DAC, Digital to analog converter; DSP, Digital signal processor; EV, Electric vehicle; GPIO, General purpose input output; IGBT, Insulated gate bipolar transistor; MLIs, Multilevel inverters; PMSM, Permanent magnet synchronous motor; PPR, Pulses per revolution; QEP, Quadrature encoder pulse; RPM, Revolutions per minute; SVD, Space vector diagram; SVM, Space vector modulation; TCHB, Transistor-clamped H bridge; THD, Total harmonic distortion; UDC, Urban driving cycle; V_{DC}, Input DC supply of each phase of TCHB inverter; C_{1a}, C_{2a}, DC link capacitors of phase "a" of TCHB inverter; S_{1a}, S_{2a}, S_{3a}, S_{4a}, S_{5a}, IGBT switches of phase "a" of TCHB inverter; D_2, D_3, D_4, D_5, Feedback diodes; D_{11}, D_{22}, D_{33}, D_{44}, Bridge diodes; N, Neutral point of the DC link capacitors in each phase of TCHB inverter; A, B, C, Load terminals of phases "a," "b," and "c" of three-phase TCHB inverter; O, Common terminal of phases "a," "b," and "c" of TCHB inverter; 1, 2, 3, 4, 5, 6, Big hexagons in the five-level SVD; A, B, C, D, E, F, Small hexagons in the five-level SVD; $PV3_1$ to $PV3_6$, Level-3 pivot vectors (which form a three-level hexagon with their tips joined and help in translation of the five-level reference vector from five level to three level); $PV2_1$ to $PV2_6$, Level 2 pivot vectors (which form a two-level hexagon with their tips joined and help in translation of the three-level reference vector from three level to two level); A1, Small hexagon A of Big Hexagon 1; D1, Small Hexagon D of Big Hexagon 1; A4, Small Hexagon A of Big Hexagon 4; D4, Small Hexagon D of Big Hexagon 4 (symbols for the other small hexagons can be interpreted accordingly); +a, Phase "a" positive axis; -a, Phase "a" negative axis; K_p, Proportional gain of the PI controller; T_i, Integral time constant of the PI controller.

REDUCED SWITCHING ANALYSIS-BASED SPACE VECTOR MODULATION ALGORITHM FOR MULTILEVEL INVERTERS

Poonam Jayal* and Gurumoorthy Bhuvaneswari*

Abstract

This paper proposes a generalized and mathematically less intensive algorithm for implementing space vector pulse-width modulation in multilevel inverters. It simplifies the space vector diagram (SVD) of a $(2^n + 1)$-level inverter, stepwise, into a basic two-level case using "n" pivot vectors and proposes a considerable reduction in the switching analysis based on a noteworthy relationship elucidated and established between the switching sequences of the various two-level hexagons of the multilevel SVD. It is proposed that the switching sequences of a $(2^n + 1)$-level inverter with 6^n two-level hexagons in its SVD can be derived by investigating the switching combinations of merely 2^n two-level hexagons, irrespective of the voltage source inverter topology, thereby reducing the memory requirements for lookup tables and the computation time of the processor considerably. The algorithm has been successfully simulated in the MATLAB/Simulink environment and experimentally verified on the laboratory prototypes of multiple multilevel topologies. Experimental implementation using a digital signal processor (DSP) with the Embedded Coder tool from Simulink toolbox obviates the need for conventional DSP programming, adding to the simplicity of the proposed algorithm.

Key Words

Cascaded H bridge inverter, multilevel inverter, neutral point clamped inverter, space vector pulse-width modulation, digital signal processor, Embedded Coder

1. Introduction

Research on multilevel inverters (MLIs) dates back to the early 1980s with the invention of a three-level neutral point clamped (NPC) inverter [1] and thereafter introduction of a generalized structure for an MLI in 1983 [2]. MLIs were developed to supersede the conventional two-level inverters for medium-voltage and high-power applications, especially for electric motor drives with variable frequency operations. With the basic underlying principle of generating a stepped voltage waveform from the available capacitor voltage levels [3], MLIs primarily target to produce an output voltage as close as possible to a sinusoidal output. The higher the levels of the MLI, the closer it is to replicating a sinusoidal output, thereby reducing the output voltage and current harmonics and developing an energy-efficient motor drive system. MLIs offer lower voltage stress across devices, thereby generating a low common-mode voltage across motor windings [4]. Several methods have been proposed for the firing of MLIs, but space vector pulse-width modulation (SVPWM) technique continues to be one of the most desirable methods for firing of MLI devices owing to its numerous merits such as reduced harmonic losses, lower switching frequencies and thus reduced switching losses, better utilization of the DC bus and easier digital implementation [5]–[7].

The vast literature on SVPWM primarily explores various algorithms to simplify the complex space vector diagram (SVD) of an MLI to primarily identify the position of the reference vector and zero in the best possible switching vectors in its proximity to finally design the optimum switching sequence for generating the inverter firing pulses. Several authors have proposed SVPWM algorithms for MLIs which decompose the n-level SVD to a basic two-level case to simplify the "ON" time calculation for the inverter switches. The SVPWM algorithm proposed in [8] maps the reference space vector (SV) from any sector of a five-level SVD to the respective sector of the innermost hexagon, which generates switching sequence corresponding to a two-level inverter. However, identifying the centre of the sub-hexagon containing the tip of the reference SV, which is the key component required for the above translation, is computationally intensive, especially for higher levels. References [9] and [10] propose SVPWM algorithms for a three- and five-level inverter, respectively, by decomposing the SVD to two-level, but the reference voltage vector correction and the generation of the switching sequences are not explained adequately. Gupta and Khambadkone [11] use a mapping algorithm for an MLI based on a two-level inverter involving multiple variables for identifying the sub-triangle containing the reference

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Space Vector Based Enhanced Modulation Scheme for a Reduced Switch Five-Level Inverter

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***Abstract*— This paper proposes a new space vector pulse width algorithm-based modulation scheme for a reduced switch five-level inverter topology, referred to as a 'Transistor-Clamped H Bridge (TCHB) inverter' in literature. This inverter topology invites attention primarily due to the considerable reduction that it offers in terms of the number of active switches used in a five-level inverter topology. It uses 15 active switches as compared to the 24 being used in a conventional five-level neutral point clamped (NPC) or cascaded H-Bridge (CHB) inverter. The proposed modulation scheme aims to enhance the performance of the TCHB inverter by offering an improved performance at lower switching frequencies, such as an output with reduced total harmonic distortion (THD) content, thereby minimizing switching losses and improving the overall inverter efficiency, paving way for its utilization for high capacity motor drive applications with huge device currents switching at a slower pace. MATLAB/Simulink based simulations and experimental results obtained from the laboratory prototype of a three-phase TCHB inverter feeding an RL load validate the efficacy of the proposed modulation scheme over the conventional carrier-based scheme. A digital signal processor (DSP) and embedded coder toolbox from MathWorks are used for simplified implementation of the space vector algorithm, while realizing the experimental prototype.**

Keywords*— *Multilevel inverter, space vector, pulse width modulation, Transistor clamped H Bridge inverter, DSP

I. Introduction

Multilevel inverters (MLIs) with reduced number of switches ensuring cost optimisation are being increasingly sought after for motor drive applications [1]-[2]. Their rising popularity has, in turn, attracted newer modulation schemes for MLIs. However, space vector pulse width modulation (SVPWM) technique continues to be one of the most desirable methods for firing of MLI devices owing to its numerous merits such as an effective utilization of the DC bus, reduced harmonic distortion even at lower switching frequencies, reduced switching losses and ease of implementation [3]-[4]. Researchers have been trying to simplify the analysis and implementation of SVPWM methodologies [5-6] to cater to the requirements of the MLIs based on their applications.

This paper revisits a five-level reduced switch inverter topology, referred to as a 'Transistor-Clamped H Bridge (TCHB) inverter' in the literature. This circuit has become popular owing to the reduced device count that it offers for attaining a five-level output voltage. It uses 15 active switches as compared to the 24 being used in a conventional five-level neutral point clamped (NPC) or cascaded H-Bridge (CHB) inverter. The single-phase configuration of the TCHB topology was introduced in [7] along with a deadbeat controller to alleviate the harmonic components in the output voltage and load current. A detailed comparison of the TCHB topology with conventional five-level inverter topologies is presented in [8]. Selvaraj et al.[9] thereafter explored this single-phase topology for a grid connected PV system comparing it with a conventional three-level grid tied PV system. A cascaded configuration of the TCHB topology for a medium-voltage drive application is explored in [10], with emphasis on the midpoint capacitor voltage balancing of each cell. It also presented a detailed comparison of the five level TCHB inverter topology with several conventional MLI topologies considering device specifications, power quality and power losses and established that, truly, TCHB inverter's efficacy is by far the best. It is proposed in [11] that the TCHB topology can easily be extended to any number of voltage levels incorporating very few active switching devices, thereby improving reliability of the system. Gautam et al. [12] have recently addressed the reliability issues of the TCHB inverter and proposed a modified topology for addressing the same. Si and SiC based hybrid configurations of the TCHB inverter have also been explored recently for high-efficiency photovoltaic applications [13].

In continuation with the ongoing research on the TCHB inverter topology, this paper explores an alternate modulation scheme for this topology. TCHB has so far been triggered only with carrier-based modulation schemes [7]-[10], which offer desirable inverter output with reduced distortion only at higher switching frequencies, incurring more switching losses and thus lowering the overall inverter efficiency. This paper proposes a reduced switching analysis based simplified space vector pulse width modulation (SVPWM) scheme for the TCHB inverter with an aim to enhance its performance at lower switching frequencies thereby making it suitable for high capacity motor drive applications operating at lower switching frequencies owing to the huge device currents. The SVM algorithms reported so far for multilevel inverters adopt the basic methodology of decomposing any n-level space vector diagram (SVD) to two-level, in order to simplify the dwell time calculation for the inverter switches [14]-[16].

The SVPWM scheme proposed in this work for the five-level TCHB inverter is based on the same principle, however, with a much-simplified switching analysis, which has been proposed based on a useful relationship deduced between the switching combinations of the various two-level hexagons of a five-level SVD. The proposed modulation scheme has been

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Simplified Sensor Based Vector Control of Permanent Magnet Synchronous Motor Drive

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***Abstract*—This paper presents a sensor-based vector control implementation for a permanent magnet synchronous motor (PMSM) drive using an encoder on a digital signal processor (DSP) platform. A built-in incremental encoder provides the necessary position and speed information for transforming three-phase stationary reference frame of the stator currents to the two-axis rotating d-q reference frame of the rotor. The use of an encoder enables easy computing of rotor position even at very low speeds, which is a major limitation of the back emf estimation based sensorless control techniques. DSP and Embedded coder toolbox of MATLAB, together with the current sensors and incremental encoder, offer a compact, cost effective and simplified system for implementation of the popular vector control technique for AC drives, as compared to a dSPACE controller-based system often discussed in the literature. Also, embedded coder toolbox minimizes the efforts while programming the DSP as the simulink model itself can be used for experimentation merely by modifying its MATLAB 'configuration parameters'. MATLAB/Simulink based simulation results for a vector controlled PMSM drive have been validated with the help of experiments performed on a 3.5 kW laboratory prototype of the PMSM drive fed from a two-level voltage source inverter controlled by sinusoidal pulse width modulation technique.**

***Index Terms*—Encoder, Vector control, PMSM, DSP, Embedded Coder**

I. Introduction

Permanent magnet synchronous motors (PMSMs) are employed in many critical applications such as aerospace systems, electric vehicles, robotics and other consumer related appliances, due to their merits over other AC machines, like compactness, higher torque to inertia ratio, fast dynamic response and remarkable efficiency [1]-[2]. Moreover, the advent of specialized digital signal processors (DSPs) with built-in modules for pulse width modulation (PWM) control, processing of encoder pulses, analog to digital signal conversions and vice versa, simplify the implementation of the control algorithms for the PMSM drive, adding to their overall popularity in the industrial domain.

Several popular control techniques have evolved for PMSMs [3], vector control being the most popular, as it offers an excellent dynamic response for low as well as high speeds. Vector control simplifies the control of an AC machine by decoupling the torque and flux producing components of the stator current using Clarke's and Park's transformations [4], thereby enabling independent torque and flux control similar to a DC machine, eliminating bandwidth and phase shift limitations of the PI controllers at high speeds. Acquiring the airgap flux position information (airgap flux angle with respect to the R phase of the stator) is the crux of vector control. It is this angle which is used for transforming the three-phase time variant system (abc reference frame) into a two-phase time invariant system (dq reference frame) to obtain the desired electromagnetic torque at a particular speed. An error in the measured or estimated rotor position leads to a reduced starting torque and a temporary reversal in rotation at motor starting [5].

Rotor position measurement has been adequately reported in literature using sensor based and sensorless estimation methods. Sensor-based rotor position measurement methods for PMSM primarily include incremental encoders [6]-[9], as they are inexpensive and provide accurate but relative rotor position information. However, by using the index pulse as a homing signal it can be used to give absolute rotor position [10]. Sensorless estimation techniques are broadly based on back emf based estimation, extended Kalman filter-based state observers and saliency-based tracking depending on magnetic saturation effects [11]-[12], high frequency signal injection and magnetic saturation voltage injection [13] based methods. Back emf based estimation method is the simplest sensorless technique for medium and high speeds, but inefficient for low speed estimation. Other estimation methods are mathematically intensive. Also, many of them are based on machine parameters, which are sensitive to changes in temperature and other ambient conditions.

Sensor based methods offer ease of rotor position measurement required for vector control of PMSM, especially with the use of the advanced DSPs with their in-built encoder signal processing modules like the quadrature encoder pulse module (QEP). They are also efficient for low speed measurements. Since vector control is known to be computationally intensive, DSPs are the most judicious choice for their implementation due to their compactness and fast processing capability.

This paper presents an incremental encoder-based simplified vector control of a 3.5 kW surface mounted PMSM drive.The use of an incremental encoder enables easier rotor position detection obviating the need for tedious calculations unlike the sensorless vector control schemes.The closed-loop vector

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Vector Control of Permanent Magnet Synchronous Motor Drive using a reduced switch five-level inverter

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***Abstract*— This paper presents one of the most popular closed-loop control techniques namely the Vector Control for the control of a Permanent Magnet Synchronous Motor (PMSM) drive using a reduced switch five-level inverter. A SIMULINK model for the vector control of a surface mounted PMSM drive system is implemented using two different inverters, namely, a conventional sinusoidal pulse width modulated (SPWM) two-level voltage source inverter (VSI) and a reduced switch five-level PWM VSI. A comparative performance analysis of the two topologies is presented, for various dynamic operating conditions like load torque perturbations and different reference speed conditions, keeping the DC link voltage and carrier frequency the same for both topologies. The simulation results of the proposed drive system using a reduced switch five-level inverter validate the relevance of the rising popularity of multilevel inverters for adjustable speed drive applications and also emphasize the fact that a five-level inverter offers an advantageous choice of working with lower switching frequencies, maintaining a low and consistent value of current THD , thereby reducing switching losses, unlike SPWM technique for the two-level VSI which needs to be implemented at higher switching frequencies in order to maintain a low value of current THD.**

Keywords—* *Vector control, Surface Mounted PMSM, SPWM, multilevel inverters

I. Introduction

Permanent Magnet Synchronous Motors are reigning the field of adjustable speed drive applications like fans, blowers, centrifugal pumps, robots, hybrid vehicles, machine tools etc. and gradually replacing the DC and induction motors in this domain. This has been possible due to the unique properties of PMSM like high torque and flux density, smaller size, high efficiency and power factor, superior dynamic performance, spark-less operation, low noise and a longer life.

Vector Control is one of the most popular closed-loop control techniques employed to obtain an excellent dynamic performance for the PMSM. It enables the separation of the torque-producing and flux-producing components of stator current, thereby providing a decoupled control for the PMSM drive emulating the control structure of a separately-excited DC machine [1-2]. Thus, vector control transforms the control of an alternating current machine into that of a DC machine by allowing independent torque and flux control. Vector control imparts complete motor torque capability to the PMSM at speed ranges below rated speed and an efficient performance over a wider speed range. DTC has a simpler structure and better dynamic performance, but its starting performance and low speed operation are known to have several problems related to torque pulsations.

Multilevel inverters primarily attempt to synthesize a sinusoidal voltage from multiple levels of voltage obtained from several levels of capacitor voltages. As the number of levels increase the output of the inverter gets closer to a sinusoidal output with a very less harmonic distortion, thereby providing a ripple free output, low harmonic losses and reduction in the torque pulsations. Multilevel inverters also provide a low dV/dt switching stress and voltage stress for each of their devices, thereby allowing lower device ratings as compared to a conventional two level SPWM inverter of similar power rating [3].

Being a synchronous machine, PMSM is usually started with a low frequency supply and is therefore mostly inverter driven unless it is started by using damper bars. A number of papers have discussed the details of conventional two level SPWM inverter fed PMSM drives. With the advent of multilevel inverters in the power industry, researchers have been trying to explore their implementation in the field of adjustable speed ac drives too [4-6]. Although the concept of multilevel inverters was introduced way back in 1981[7], they continue to dominate the research interests of many owing to the innumerable benefits that they have to offer.

One of the most popular multilevel inverter topologies is the cascaded H bridge (CHB) topology. In order to implement a five-level inverter, a CHB circuit would require 24 switches. This paper presents an alternate five-level inverter topology with 15 switches [8-10] which is a cost-effective alternative to the conventional five-level CHB inverter. This paper also presents an effective strategy for implementation of vector control of a PMSM with this reduced switch five-level inverter topology. A comparative analysis of the vector control with conventional two-level SPWM and using the reduced switch five-level inverter has been done based on the simulations carried out on the proposed drive system in MATLAB/ Simulink environment.

II. Mathematical Modeling of a PMSM

The dynamic model of a surface mounted PMSM is developed in the d-q reference frame, based on the following mathematical equations [11] and assuming PMSM to be

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